

10715593\_QUAL.txt

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PLUS Search Results for S/N 10715593, Searched March 10, 2005

The Patent Linguistics Utility System (PLUS) is a USPTO automated search system for U.S. Patents from 1971 to the present. PLUS is a query-by-example search system which produces a list of patents that are most closely related linguistically to the application searched. This search was prepared by the staff of the Scientific and Technical Information Center, SIRA.

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with 16  
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would 4  
written 1

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Most Frequently Occurring Classifications of Patents Returned  
From A Search of 10715593 on March 10, 2005

Original Classifications

3 711/122  
2 123/406.32  
2 703/19  
2 712/213  
2 712/244

Cross-Reference Classifications

4 711/118  
3 711/141  
3 711/144  
3 711/145  
2 702/186  
2 703/21  
2 710/260  
2 711/117  
2 711/119  
2 711/120  
2 711/121  
2 711/122  
2 711/203  
2 712/23  
2 712/24

Combined Classifications

5 711/122  
4 711/118  
4 711/141  
3 710/260  
3 711/144  
3 711/145  
3 712/213  
2 123/406.32  
2 375/293  
2 702/186  
2 703/19  
2 703/21  
2 711/117  
2 711/119  
2 711/120  
2 711/121  
2 711/203  
2 712/22  
2 712/23  
2 712/24  
2 712/244

Titles of Most Frequently Occurring Classifications of Patents Returned  
From A Search of 10715593 on March 10, 2005

- 5 711/122 (3 OR, 2 XR)  
Class 711 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING  
SYSTEMS: MEMORY  
711/100 STORAGE ACCESSING AND CONTROL  
711/117 .Hierarchical memories  
711/118 ..Caching  
711/119 ...Multiple caches  
711/122 ....Hierarchical caches
- 4 711/118 (0 OR, 4 XR)  
Class 711 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING  
SYSTEMS: MEMORY  
711/100 STORAGE ACCESSING AND CONTROL  
711/117 .Hierarchical memories  
711/118 ..Caching
- 4 711/141 (1 OR, 3 XR)  
Class 711 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING  
SYSTEMS: MEMORY  
711/100 STORAGE ACCESSING AND CONTROL  
711/117 .Hierarchical memories  
711/118 ..Caching  
711/141 ...Coherency
- 3 710/260 (1 OR, 2 XR)  
Class 710 : ELECTRICAL COMPUTERS AND DIGITAL DATA  
PROCESSING SYSTEMS: INPUT/OUTPUT  
710/260 INTERRUPT PROCESSING
- 3 711/144 (0 OR, 3 XR)  
Class 711 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING  
SYSTEMS: MEMORY  
711/100 STORAGE ACCESSING AND CONTROL  
711/117 .Hierarchical memories  
711/118 ..Caching  
711/141 ...Coherency  
711/144 ....Cache status data bit
- 3 711/145 (0 OR, 3 XR)  
Class 711 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING  
SYSTEMS: MEMORY  
711/100 STORAGE ACCESSING AND CONTROL  
711/117 .Hierarchical memories  
711/118 ..Caching  
711/141 ...Coherency  
711/145 ....Access control bit
- 3 712/213 (2 OR, 1 XR)  
Class 712 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING  
SYSTEMS: PROCESSING ARCHITECTURES AND INSTRUCTION  
PROCESSING  
712/209 .Decoding instruction to accommodate plural  
instruction interpretations (e.g., different dialects,  
languages, emulation, etc.)  
712/213 .Predecoding of instruction component
- 2 123/406.32 (2 OR, 0 XR)  
Class 123 : INTERNAL-COMBUSTION ENGINES  
123/406.11 SPARK IGNITION TIMING CONTROL



- 123/406.12 .Electronic control
- 123/406.19 ..Closed loop feedback control of spark timing
- 123/406.26 ...Combustion condition responsive
- 123/406.29 ....Engine knock responsive
- 123/406.3 .....Fuel quality or composition signal responsive
- 123/406.32 .....Having a plurality of speed/load maps related to fuel quality or composition
- 2 375/293 (1 OR, 1 XR)
  - Class 375 : PULSE OR DIGITAL COMMUNICATIONS
  - 375/286 MULTILEVEL
  - 375/293 .Synchronized
- 2 702/186 (0 OR, 2 XR)
  - Class 702 : DATA PROCESSING: MEASURING, CALIBRATING, OR TESTING
  - 702/127 MEASUREMENT SYSTEM
  - 702/182 .Performance or efficiency evaluation
  - 702/186 ..Computer and peripheral benchmarking
- 2 703/19 (2 OR, 0 XR)
  - Class 703 : DATA PROCESSING: STRUCTURAL DESIGN, MODELING, SIMULATION, AND EMULATION
  - 703/13 SIMULATING ELECTRONIC DEVICE OR ELECTRICAL SYSTEM
  - 703/19 .Timing
- 2 703/21 (0 OR, 2 XR)
  - Class 703 : DATA PROCESSING: STRUCTURAL DESIGN, MODELING, SIMULATION, AND EMULATION
  - 703/13 SIMULATING ELECTRONIC DEVICE OR ELECTRICAL SYSTEM
  - 703/21 .Computer or peripheral device
- 2 711/117 (0 OR, 2 XR)
  - Class 711 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MEMORY
  - 711/100 STORAGE ACCESSING AND CONTROL
  - 711/117 .Hierarchical memories
- 2 711/119 (0 OR, 2 XR)
  - Class 711 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MEMORY
  - 711/100 STORAGE ACCESSING AND CONTROL
  - 711/117 .Hierarchical memories
  - 711/118 ..Caching
  - 711/119 ...Multiple caches
- 2 711/120 (0 OR, 2 XR)
  - Class 711 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MEMORY
  - 711/100 STORAGE ACCESSING AND CONTROL
  - 711/117 .Hierarchical memories
  - 711/118 ..Caching
  - 711/119 ...Multiple caches
  - 711/120 ....Parallel caches
- 2 711/121 (0 OR, 2 XR)
  - Class 711 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MEMORY
  - 711/100 STORAGE ACCESSING AND CONTROL

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711/117      .Hierarchical memories
711/118      ..Caching
711/119      ...Multiple caches
711/121      ....Private caches

2  711/203      (0 OR, 2 XR)
    Class 711 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING
                SYSTEMS: MEMORY
711/200      ADDRESS FORMATION
711/202      .Address mapping (e.g., conversion,
                translation)
711/203      ..Virtual addressing

2  712/22      (1 OR, 1 XR)
    Class 712 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING
                SYSTEMS: PROCESSING ARCHITECTURES AND INSTRUCTION
                PROCESSING
712/1        PROCESSING ARCHITECTURE
712/10       .Array processor
712/16       ..Array processor operation
712/22       ...Single instruction, multiple data (SIMD)

2  712/23      (0 OR, 2 XR)
    Class 712 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING
                SYSTEMS: PROCESSING ARCHITECTURES AND INSTRUCTION
                PROCESSING
712/1        PROCESSING ARCHITECTURE
712/23       .Superscalar

2  712/24      (0 OR, 2 XR)
    Class 712 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING
                SYSTEMS: PROCESSING ARCHITECTURES AND INSTRUCTION
                PROCESSING
712/1        PROCESSING ARCHITECTURE
712/24       .Long instruction word

2  712/244      (2 OR, 0 XR)
    Class 712 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING
                SYSTEMS: PROCESSING ARCHITECTURES AND INSTRUCTION
                PROCESSING
712/220      PROCESSING CONTROL
712/233      .Branching (e.g., delayed branch, loop control,
                branch predict, interrupt)
712/244      ..Exception processing (e.g., interrupts and
                traps)

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